AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning on page 21, line 6, as follows:

This delay circuit is derived from the delay circuit shown in Figure 2B, and by providing ~~NAND~~ NOR-gates V43, V45 on the transmission path of the delay circuit, the circuit is designed so that, when the logic signal reverts to the high level, the internal state of the delay circuit is returned rapidly to the original state.

Please amend the paragraph beginning on page 21, line 10, as follows:

In the diagram shown, the inverters V41, V42 and the n-MOS transistor N41 of high-Vt construct a delay path based on the same concept illustrated in Figure 2B, and the delay circuit operates by delaying a logic signal SIN and inputting the signal into one input section of the ~~NAND~~ NOR-gate 43. The other input section of the ~~NAND~~ NOR -gate 43 receives the logic signal SIN directly. The ~~NAND~~ NOR -gate 43, n-MOS transistor N42 of high-Vt and the inverter V44 also construct a delay circuit based on the concept illustrated in Figure 2B, and the delay circuit operates by delaying a logic signal SIN and inputting the signal into one input section of the ~~NAND~~ NOR -gate 45. The other input section of the ~~NAND~~ NOR -gate 45 receives the logic signal SIN directly. The output signal from the ~~NAND~~ NOR -gate 45 is input in the inverter V46 and is output as signal SOUT.

Please amend the paragraph beginning on page 22, line 1, as follows:

In Embodiment 4, the logic signal SIN is at the high level in the initial stage, and when the logic signal changes from this state to the low level, this logic signal SIN transmits through the delay circuit comprised by the inverter 41, n-MOS transistor N41 and inverter V42, and through the delay circuit comprised by the ~~NAND~~ NOR -gate V43, n-MOS transistor N42 and inverter V44, and is input in the ~~NAND~~ NOR -gate V45, and transmits through the ~~NAND~~ NOR -gate V45 and the inverter V46 to be output as signal SOUT. In this manner, the logic signal SIN is delayed and is output as signal SOUT.

Please amend the paragraph beginning on page 22, line 8, as follows:

In contrast, when the logic signal SIN changes from the low level to the high level, the output signal from the ~~NAND~~ NOR -gates V43, [[V44]] V45 is forced to the low level, and the internal state of the delay circuit is quickly reverted to the initial state.